REMARKS

Reconsideration is requested in view of the above amendments and the following remarks. The specification has been amended to describe the reference character 73 as a multi-route switch shown in Figure 7. The specification also has been amended editorially to better reflect the description of Figure 5 in the original PCT publication, which was published in Chinese. Claims 1-3, 6, 8-10 and 13-18 have been revised. Claim 7 has been canceled without prejudice or disclaimer. Support for the revisions can be found at, e.g., original claim 7, page 3, line 19, the second and third full paragraphs on page 7 of the specification, and Figs. 5 and 7. Claims 1-6 and 8-18 remain pending in the application.

Drawings

Figure 1 is designated as "Prior Art". The reference character 73 is described in the amended specification as a multi-route switch. Figure 4 includes the features of the invention specified in claim 1. In particular, Step 150 includes the feature of waiting for an exiting signal from the command in the pipeline being sent during a pipeline period immediately before a last cycle of a command exiting the pipeline. Step 180 includes the features in the "wherein" clause as recited in claim 1, and shows inserting an instruction after receiving an exiting signal from the command in the pipeline before it exits the pipeline. Regarding Figure 5, this figure shows an example of the overlapping submitting method as described in the second full paragraph on page 5 of the specification. In the overlapping method, a new command is inserted in the last cycle of a certain command in which the certain command will exit the pipeline. Figure 5 shows Command A as being in the last cycle of a cycle operation. Command G is inserted in this last cycle, and before Command A exits at the third pipeline stage, Command A and Command G execute in parallel. Then, Command A exits at the third pipeline stage and Command G exits at the sixth pipeline stage. That is to say, due to the cycle operation of Command A, the sequence of commands entering the pipeline (Command G) may be inconsistent with the sequence of commands exiting the pipeline (Command A) after the completion of the performance. It is in this sense that the command submitting method

of claim 1 can be understood as being an overlapping command submitting method of dynamic cycle pipeline. Thus, contrary to the rejection's position, Figure 5 describing an overlapping command submitting method of dynamic cycle pipeline is supported by the specification and is not contrary to the claims and the invention. Regarding the exiting signal being released two stages before the new command enters the pipeline, Applicants submit that this feature can be understood from the last full paragraph of page 6 of the specification and Figure 5. That is, as indicated above, Figure 5 shows Command A in the last cycle of a cycle operation, where Command G is inserted at the No. 1 pipeline stage and Command A exits at the third pipeline stage. Thus, two stages before Command G is inserted is released can be at a pipeline stage one pipeline period before the last cycle of the cycle operation of Command A, and in particular, the fifth stage of the one pipeline period before the last cycle of the cycle operation of Command A. Step 180 of Figure 4 includes features from original claim 7, which is now incorporated into claim 1. The figures also have been amended to address the issues raised in items 8, 9 and 10 of the Office Action.

Claim Objections

As to claim 1, amended claim 1 does not recite "wherein a command exits the pipeline at a predetermine stage without passing through stages subsequent to the predetermined stage in the pipeline". Claims 1, 2, 3, 7, 8, 9, 10 and 13-18 were amended, taking into account the issues noted in the objections, and in items 12-21 of the Office Action. Withdrawal of the objection is requested.

Claim Rejections – 35 USC § 112

Claims 3, 5, 7-8, 10 and 13-18 are rejected under 35 USC 112, second paragraph, as being indefinite. As to claim 7, the features in claim 7 are now incorporated into claim 1. Claim 1 recites that the new command and the old command each contain a field, and the step of determining whether there is any field conflict between the new command and the old command. As to claim 10, claim 10 recites an "operator processing unit". Claim 10 further recites "the" dynamic cycle pipeline, thereby referring back to the "dynamic

cycle pipeline" recited in the preamble of claim 1. Claims 13-18 were amended to track the revisions to claim 10. Claims 3, 5 and 8 were amended, taking the issues noted in the rejection into account. Applicants respectfully submit that the claims are definite and request that the rejection be withdrawn.

Claim Rejections – 35 USC § 102

Claims 1, 4-10 and 15-18 are rejected under 35 USC § 103(a) as being anticipated by Computer Organization and Design (hereinafter referred to as "Hennessy"). Applicants respectfully traverse this rejection.

Claim 1 has been amended to include the subject matter of claim 7, as well as the details suggested by the Examiner. In particular, claim 1 recites that the new command and the old command each contain a field. Claim 1 further recites that step (e) includes determining whether there is any field conflict between the new command and the old command, and if there is any field conflict between the new command and the old command, then a field branch is created, the field branch including a major current register for storing the field of the new command and a branch current register for storing the field of the old command, the field of the new command being added into the pipeline when submitting, and the field of the old command being entered into the branch current register and maintained in the field branch until the old command uses the field for the last time. Claim 1 further recites that the major current register and the branch current register are connected to a hardware processing module through a multi-route switch. If the new command is processed by the hardware processing module, the hardware processing module receives an input of the major current register in which the field of the new command is stored, and if the old command is processed by the hardware processing module, the hardware processing module receives an input from the branch current register in which the field of the old command is stored. Claim also recites that if there is no field conflict, a field switch is conducted in a corresponding pipeline segment after submitting. As recognized by the rejection, Hennessy does not teach or suggest these features. Therefore, claim 1 and its dependent claims are patentable over Hennessy.

Claim Rejections – 35 USC § 103

Claims 2, 3 and 11-14 are rejected under 35 USC 103(a) as being unpatentable over Hennessy, and further in view of US 5084814 to Vaglica. Claim 1 includes features from original claim 7, which was not included in this rejection. Claim 1 also includes features supported at the second and third full paragraphs on page 7 of the specification. Claims 2, 3 and 11-14 depend from claim 1. Therefore, the rejection is rendered moot. Applicants do not concede the correctness of the rejection.

In view of the above amendments and remarks, Applicants believes that the pending claims are in a condition for allowance. Favorable reconsideration is respectfully requested. If any questions arise regarding this communication, the Examiner is invited to contact Applicants' representative listed below.

Respectfully submitted,

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